Surface Mounted (SMD) TCXO

Available in 7x5mm- 5x3mm - 3x2mm - 2.5x2mm Package

TTL/CMOS Compatible Output TCXO

RoHS compliant 2002/95/EC

Static sensitive device

Current part - Recommended for new designs

Op. Temp Range	Frequency Stability (PPM)					
	±0.5	±1.0	±1.5	±2.0	±2.5	±3.0
0°C to +50°C	✓	✓	✓	✓	✓	✓
-10°C to +60°C	Δ	✓	✓	✓	✓	✓
-20°C to +70°C	×	✓	✓	✓	✓	✓
-30°C to +75°C	×	✓	✓	✓	✓	✓
-40°C to +85°C	×	Δ	Δ	✓	✓	✓

Δ= Contact AEL

Storage Temp.	-55°C to +125°C

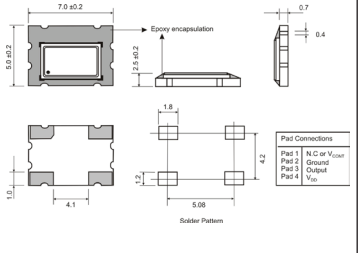
Supply Voltage	Option Code
+3.3V DC	3
+2.8V DC	28
+2.5V DC	25
+1.8V DC	18

Marking & Specification Code Format

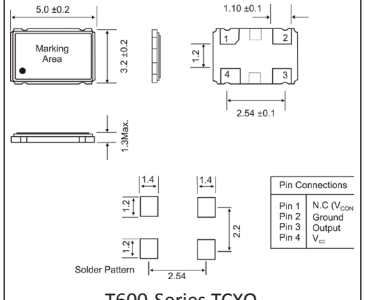
Type	Voltage Code	Temp Range/Stability Options	WWYY
T***	3,28,25 or 18	See table above	1611

Parameter	Condition	Value			
Available Frequency Range		4.00 - 54.00 MHz			
Initial Calibration		± 2.0 PPM			
Frequency Stability	vs Temperature	± 0.5 PPM to ± 3.0 PPM (To be specified)			
	vs Ageing	±1PPM (1st Year)			
	vs Voltage Change	±0.3PPM for ±5% Voltage change			
	vs Load Change	±0.3PPM for ±10% load change			
	vs Reflow	±1PPM after 1 reflow measured after 24hours			
Output Voltage	Peak to Peak	TTL/CMOS			
Input Current		+3.3V DC	+2.8V DC	+2.5V DC	+1.8V DC
	4.00 - 10.00 MHz	4.0mA	3.4mA	3.1mA	3.1mA
	10.01 - 20.00 MHz	4.8mA	4.1mA	3.7mA	3.7mA
	20.01 - 30.00 MHz	5.5mA	4.7mA	4.2mA	4.2mA
	30.01 - 40.00 MHz	6.0mA	5.2mA	4.6mA	4.6mA
	40.01 - 54.00 MHz	7.0mA	6.0mA	5.5mA	5.5mA
Output Load	Logic High "1"	90% VDD Min.			
	Logic Low "0"	10% VDD Max.			
Duty Cycle	at 50% V_{DD}	50% ±10%			
Rise/Fall Time	0.1VDD to 0.9VDD	10nS Max from 20% to 80% of waveform			
Start Up Time	0V to V_{DD}	10mS Max.			
Output Load	HCMOS Load	15pF Max.			
SSB Phase Noise at 25°C	**Offset**	**10Hz**	**100Hz**	**1kHz**	**10kHz**	**100kHz**
	10.000000 MHz	-115dBc/Hz	-135dBc/Hz	-148dBc/Hz	-152dBc/Hz	-155dBc/Hz
Jitter	Period jitter RMS	3ps Typ.			
Ageing	per Year at 25°C	±1PPM Max.			

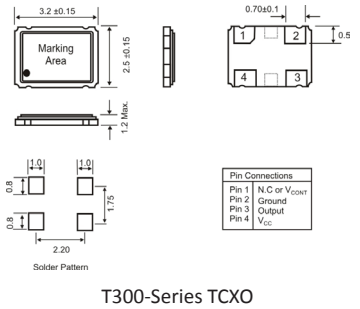
Dimensions (mm)



T430-Series TCXO



T600-Series TCXO



T300-Series TCXO